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Substitute Appellant's Brief Under 37 C.F.R. § 1.192
Appendix A-C

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Docket No.: 20136-00305-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Roy C. (deceased), Flaker et al.

Application No.: 09/588,351 Confirmation No.: 8116

Filed: June 7, 2000 Art Unit: 2815

For: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES Examiner: J. A. Fenty

SUBSTITUTE APPELLANT'S BRIEF UNDER 37 C.F.R. § 1.192

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This substitute brief is in furtherance of the following: the Notice of Appeal, filed in this case on June 18, 2004; Appellant's Brief filed August 18, 2004; the non-final Office Action mailed by the Examiner on November 30, 2004; the Request for Reinstatement of the Appeal and Supplemental Appeal Brief, filed March 30, 2005; the Notice of Non-Compliance under 37 CFR §41.37, mailed by the Examiner on November 25, 2005; and the Notice of Non-Compliance under 37 CFR §41.37, mailed by the Examiner on March 8, 2006.

This Substitute Appellant's Brief is filed to replace: the Appellant's Brief, filed August 18, 2004; the Supplemental Appeal Brief, filed March 30, 2005; and the Substitute Appellant's Brief, filed December 27, 2005.

Although no fees are believed to be required for filing this brief, if any fees are required, authorization is hereby granted to charge CBLH Deposit Account No. 22-0185.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest

The real party in interest is the International Business Machines Corporation, Assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences known to the undersigned which will directly effect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-5 have been cancelled.

Claims 6-14 are pending in the application.

Claim 15 is withdrawn from consideration.

Claims 6-14 are rejected and are on appeal.

IV. Status of Amendments

There are no unentered amendments filed subsequent to the Rejection mailed on November 30, 2004.

V. Summary of Invention

The invention provides a method for enhancing the performance of an SOI device. As shown in FIG. 2, an SOI device includes a substrate 210, and an insulating layer 220. Devices are fabricated above the insulation layer 220. The advantage of the structure is disclosed in the specification, particularly on page 2 beginning at line 18 thereof, wherein SOI devices are described as typically having lower parasitic capacitances. This means that SOI devices can provide faster switching times. As described on page 3 beginning at line 21, the SOI device can accumulate electric charge on the body (the region of the MOSFET between the source and the drain). The increased charge can adversely effect the operation of the circuit, notably switching speed.

The present invention, as embodied in the circuit of FIG. 3 provides for discharging this accumulated charge. In operation, transistor 360 acts as a switch interconnecting circuits 320 and 330 whenever operation signal 350 is activated. The pulse discharge circuit 310 enhances the switching speed of transistor 360, by, just prior to activating the operation signal 350, discharging the accumulated charge from transistor 360 to reference ground 370.

FIG. 6 shows a practical embodiment wherein word line drivers 430, 440 are discharged prior to accessing a word line. When the segment driver 450 is activated, the same control signal (CTL) is used to select one of the memory subarrays or segments for writing, and is also used as an input to the pulse discharge circuit 310. The activated pulse discharge circuit 310 pulls each of transistors 432, 435, etc. to a reference ground discharging the accumulated charge on the

memory subarray just prior to selection of the subarray for access. The foregoing initializes the subarray so that it can be accessed at a greater speed.

VI. Issues

The issues on appeal are:

1. Are claims 6, 8, 9, 11 and 14 properly rejected under 35 U.S.C. § 102(e) as being anticipated by Okumura et al. (U.S. Pat. No. 5,892,260); and

2. Are claims 7, 10, 12 and 13 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Okumura et al. (U.S. Pat. No. 5,892,260) in view of Ohmi (U. S. Pat. No. 4,907,053)?

VII. Grouping of Claims

Claims 6-7 and 9-12 stand and fall together.

Claim 8 stands and falls alone.

VIII. Arguments

<u>The Rejection of Claims 6, 8, 9, 11 and 14 Under 35 U.S.C. § 102(e) as being Anticipated by U.S. Patent No. (5,892,260) Is in Error.</u>

The claimed invention is directed to methods for enhancing the performance of an SOI semiconductor device. It is possible for a charge to accumulate on the body of SOI devices which reduces there switching speed. Thus, the claimed methods call for discharging of the SOI device prior to accessing it, so that the speed of switching can be maximized.

In accordance with the Applicant's rejected claim 6, circuit performance is enhanced by the steps of a) providing a pulse discharge circuit connected to at least one SOI device, and b) using the pulse discharge circuit to discharge any accumulated potential on a body of at least one SOI device prior to accessing the at least one SOI device. Similarly, claim 9 specifically refers to selectively grounding the body of the SOI device to dissipate charge accumulated in the body prior to accessing the device. Claims 11 likewise refers to discharging accumulated potential on the body of the SOI device to a point having lower potential than the accumulated potential prior to accessing the device. Claim 14 similarly recites discharging accumulated charge from the body of the SOI device to a reference point having lower potential than the accumulated charge prior to reading an output of the SOI device.

Anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims. *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985). There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. § 102. *Scripps Clinic and Research Foundation v. Genetech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991). In view of the foregoing authority, the cited references fail to support the asserted rejection.

The Okumura et al. (U.S. Pat. No. 5,892,260) patent fails to disclose the claimed process. Okumura et al. does not disclose any type of pulse discharge circuit, nor does it disclose that feature of Applicant's method which requires that the body be discharged <u>prior</u> to access, as recited in the claims at issue.

The entire thrust of the Okumura et al. invention is summarized in col. 4, lines 5-14 as follows:

> The threshold voltage V_{thn} is dependent upon a back gate voltage, i.e., the substrate voltage V_{subn}, as shown in FIG. 2. That is, the higher the substrate voltage V_{subn}, the lower the threshold voltage V_{thn}. Therefore, in an active mode, the substrate voltage V_{subn} is positive to lower the threshold voltage V_{thn}, so that the operation speed is increased and the power dissipation is increased. On the other hand, in a standby mode, the substrate voltage V_{subn} is zero to raise the threshold voltage V_{thn}, so that the sub threshold current is

> decreased to decrease the power dissipation and the operation speed is decreased.

Okumura et al. provides for a bias voltage generator 312 to bias the back gate region of a P-channel transistor to the supply voltage V_{DD}. This increases the absolute value of the threshold voltage V_{thn} for the device, and when the active mode is entered, the bias voltage generating circuit causes a voltage of the back gate region 305 to be at a voltage V_1 which is lower than V_{DD} and higher than V_{DD}-V_F. The result is a decrease in the absolute value of the threshold (see in particular col. 6, lines 17-27). There is no effective way of discharging the body of the device prior to access. The reference fails to disclose anywhere the advantages of discharging any accumulated potential on the body of an SOI device. Accordingly, the feature of Applicant's claimed method that requires accumulated potential to be discharged prior to accessing the SOI device is not suggested in the reference.

The Office Action of November 30, 2004, on page 3 thereof characterizes the Okumura et al. reference as follows:

> Providing a pulse discharge circuit (312, 2103) connected to the at least one SOI device; and using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device (col. 6, lines 28-37, col. 11, lines 50-67).

The cited passages of the reference disclose a voltage bias circuit 312 shown in the figures. The bias circuit establishes a "standby mode" which increases the threshold voltage for an FET by applying a bias voltage to a back gate of the FET. Col. 11, lines 50-67, and col. 12, lines 1-19.

From the description in col. 12, lines 20-26, and with reference to FIGS. 22A-22E, it appears that the substrate voltage is grounded. When the device is switched from standby to active, the back gate voltage is increased. As described above, claims 6, 9, 11 and 14 all refer specifically to removing charge on a substrate by connecting the substrate to ground prior to accessing the device. It is not seen where the cited passages suggest removing charge from the substrate. The reference is directed to changing the threshold voltage of a device, and not for removing accumulated charge prior to access to speed-up operation.

The Okumura et al. process does not seek to reduce any accumulated charge, as is provided by the pulse generator in accordance with the present invention. Since the subject matter of the reference is directed to portable electronic apparatus, and conserving power, the standby mode is used with the voltage biasing to reduce power consumption in the standby mode. The switching from a standby mode to an active mode does not suggest a pulse generation technique which discharges accumulated charge prior to switching the SOI device. It is submitted that biasing the substrate of a device in a standby mode for minimizing power dissipation, and for lowering a threshold voltage in an active mode such that it responds to a rapid switching signal, are not identical to discharging potential on a body before accessing an SOI device.

Claim 8 includes a further limitation which is not disclosed in Okumura et al. (U.S. Pat. No. 5,892,260). Specifically, claim 8 requires a delay element be coupled to the input signal. An output signal coupled to the input signal drives the circuit operation. Thus, the circuit operation is delayed until such time as the body of the device can be discharged. The use of the delay element for making certain that the circuit is initialized, by discharging accumulated charge, is not shown or disclosed in Okumura et al.

Claim 9 includes the limitations of selectively grounding at least on the plurality of SOI devices. This process step is also not shown or disclosed in the Okumura et al. patent.

The Rejection of Claims 7, 10, 12 and 13 under 35 U.S.C. §103(a) as being Unpatentable over Okumura et al. (U.S. Pat. No. 5,892,260) in view of Ohmi (U.S. Pat. No. 4,907,053) Is in Error.

The Office Action of November 30, 2004, cites a reference to Ohmi (U.S. Pat. No. 4,907,053) which allegedly in combination with Okumura et al. renders the subject matter of claims 7, 10, 12 and 13 unpatentable. It is noted that to establish a prima facie case of obviousness under Section 103, all claim limitations of a claimed invention must be taught or suggested by the prior art. See MPEP, Section 2143.03 and *In re Royka*, 490

F.2d 981, 180 USPQ 580 (CCPA 1974). In view of the foregoing authority, the cited references fail to support the asserted rejection.

The Examiner alleges that lines 33-35 of Ohmi discloses using a pulse circuit. In referring to this portion of the reference, a description is provided regarding the channel length versus the potential barrier height. It is submitted that there is nothing in this portion of the reference which refers to any pulse circuit or pulse applied to discharge accumulated charge. Ohmi is directed to a particular type of insulated gate transistor which serves as a driving transistor, without any reference to discharging accumulative charge prior to accessing the device. Thus, the combination of the teachings of Okumura et al. and Ohmi does not render claims 7, 10, 12 and 13 obvious.

IX. Summary

The Rejection mailed on November 30, 2004 fails to establish anticipation under 35 U.S.C. § 102 or make a *prima facie* case of obviousness under 35 U.S.C. § 103. As has been shown above, claims 6, 8, 9, 11 and 14 are not anticipated since not every element of the claims can be found in the cited patent to Okumura et al. (U.S. Pat. No. 5,892,260). Claims 7, 10, 12 and 13 are not obvious because the combined disclosures of Okumura et al. (U.S. Pat. No. 5,892,260) and Ohmi (U.S. Pat. No. 4,907,053) fail to teach or suggest every element of the claims.

X. Claims Involved In The Appeal

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on April 26, 2004.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0458, under Order No. 20136-00305-US from which the undersigned is authorized to draw.

Dated: April 7, 2006

Respectfully submitted,

By

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/588,351

6. (Previously presented) In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device;

using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device.

7. (Original) The method of claim 6 wherein the circuit comprises a memory circuit.

8. (Original) The method of claim 6 wherein the pulse discharge circuit comprises:

an input signal;

a delay element coupled to the input signal; and

an output signal coupled to the input signal, the output signal driving the circuit.

9. (Previously presented) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

selectively grounding the body of at least one of the plurality of SOI devices to dissipate an electric charge accumulated in the body of the at least one of the plurality of SOI devices before accessing said SOI devices.

10. (Original) The circuit of claim 9 wherein the plurality of SOI devices comprises a memory circuit.

11. (Previously presented) In a circuit comprising a plurality of SOI devices, wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator connected to the circuit;

using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator prior to accessing said at least one SOI devices.

12. (Original) The method of claim 11 wherein the plurality of SOI devices comprises a memory circuit.

13. (Original) The method of claim 12 wherein the pre-determined time is just prior to accessing the memory circuit for reading or writing data.

14. (Previously presented) A method for discharging accumulated charge from a body of an SOI device and accessing the SOI device, comprising:

generating a pulse;

using the generated pulse to provide a conductive path from the body of the SOI device to a reference point having a lower potential than the accumulated charge;

discharging the accumulated charge from the body of the SOI device to the reference point;

providing a control signal which enables access to the SOI device; and

reading an output of the SOI device,

wherein said steps of generating a pulse and discharging the accumulated charge occur prior to said step of reading an output of the SOI device.

APPENDIX B

Evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied on upon by the Examiner:

NONE

APPENDIX C

Related proceedings in connection with the Appeal:

NONE